IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **PARENT et al.**	
Serial No.: **10/799,742**	Group Art Unit: **2827**
Filed: **March 12, 2004**	Examiner: **Mai, Son Luu**
Title: **Method and Circuit for Reducing Defect Current From Array Element Failures in Random Access Memories**	
Attorney Docket No.: **CD03011**	

Entry is approved SM 03/1/06

AMENDMENT AFTER FINAL ACTION
(37 C.F.R. §1.116)

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

A. Introductory Comments

The following is submitted in response to the FINAL Office Action dated October 31, 2005 and is currently due February 28, 2006, with a one month extension.

03/01/2006 SDENBOB1 00000066 502087 10799742
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37 C.F.R. §1.8

I hereby certify that this correspondence is being

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